WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit designing apparatus for automatically generating a pattern of a semiconductor integrated circuit under control of a computer, said apparatus comprising:

an input means for inputting gate level logic circuit information, standard cell library information, and package information of a circuit block as a constituent of the semiconductor integrated circuit;

a noise analysis means for performing noise analysis for the circuit block using the information inputted by the input means;

a noise judgement means for judging whether the amount of noise that occurs in the circuit block is within a predetermined range or not, on the basis of a result of noise analysis by the noise analysis means;

a processing ending means for ending the automatic generation of the pattern of the semiconductor integrated circuit, when it is judged by the noise judgement means that the amount of noise is within the predetermined range;

a logic gate selection means for selecting a logic gate in the circuit block, which logic gate generates an amount of noise larger than a predetermined amount of noise, when it is judged by the noise judgement means that the amount of noise in the circuit block is out of the predetermined range; and

a bypass condenser addition means for adding a bypass condenser for reducing power supply noise and substrate noise to

the selected logic gate.

2. A semiconductor integrated circuit designing apparatus as defined in Claim 1, wherein the noise analysis means creates a data table on which at least one of a current waveform of a power supply current and a current waveform of a substrate current is recorded, which current waveforms are obtained when the input pattern of each logic gate in the circuit block and the capacitance of a bypass condenser incorporated in the logic gate are changed, and performs noise analysis using the created data table.

3. A semiconductor integrated circuit designing apparatus as defined in Claim 1, wherein the logic gate selection means selects a logic gate which generates a maximum amount of noise in the circuit block, on the basis of a result of noise analysis.

4. A semiconductor integrated circuit designing apparatus as defined in Claim 1, wherein the logic gate selection means calculates a noise influence level which is a degree of influence of noise that occurs in each logic gate in the circuit block, using the inputted information and floor plan information of the semiconductor integrated circuit, and selects a logic gate having a maximum noise influence level.

5. A semiconductor integrated circuit designing apparatus for automatically generating a pattern of a semiconductor integrated circuit under control of a computer, said apparatus comprising:

an input means for inputting gate level logic circuit information, standard cell library information, and package information of a circuit block as a constituent of the semiconductor integrated circuit;

a noise estimation means for estimating an amount of noise that may occur in the circuit block, using the information inputted by the input means;

a capacitance constraint designation means for designating a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to restrict the amount of noise within a predetermined range, on the basis of a result of estimation by the noise estimation means;

a comparison means for comparing an on-chip capacitance that is a capacitance of a bypass condenser incorporated in the circuit block, with the capacitance constraint;

a processing ending means for ending the automatic generation of the pattern of the semiconductor integrated circuit, when the on-chip capacitance is larger than the capacitance constraint in the comparison by the comparison means;

a logic gate selection means for selecting a logic gate in

the circuit block, which logic gate generates an amount of noise equal to or larger than a predetermined amount of noise, when the on-chip capacitance is equal to or smaller than the capacitance constraint in the comparison by the comparison means; and

a bypass condenser addition means for adding a bypass condenser to the logic gate selected by the logic gate selection means.

6. A semiconductor integrated circuit designing apparatus as defined in Claim 5, wherein the logic gate selection means calculates a noise influence level which is a degree of influence of noise that occurs in each logic gate in the circuit block, using the inputted information and floor plan information of the semiconductor integrated circuit, and selects a logic gate having a maximum noise influence level.

7. A semiconductor integrated circuit designing apparatus for automatically generating a pattern of a semiconductor integrated circuit under control of a computer, said apparatus comprising:

an input means for inputting functional specification information of a logic circuit block as a constituent of the semiconductor integrated circuit, standard cell library information of the logic circuit block, and a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass

condenser is to be incorporated in the circuit block to restrict the amount of noise within a predetermined range;

a gate level conversion means for converting the functional specification information of the logic circuit into gate level logic circuit information on the basis of functional levels;

a mapping means for performing a mapping process of assigning cells in the standard cell library information to all logic gates in the gate level logic circuit, respectively;

a comparison means for comparing an on-chip capacitance which is a capacitance of a bypass condenser that is incorporated in the logic circuit subjected to the mapping by the mapping means, with the capacitance constraint;

a processing ending means for ending the automatic generation of the pattern of the semiconductor integrated circuit, when the on-chip capacitance is larger than the capacitance constraint in the comparison by the comparison means;

a logic gate selection means for selecting a logic gate which generates an amount of noise larger than a predetermined amount of noise, when the on-chip capacitance is smaller than the capacitance constraint in the comparison by the comparison means; and

a mapping change means for assigning, in place of the mapping cell assigned in the mapping process, another cell that is equivalent in logic to the mapping cell and has an internal bypass condenser having a different capacitance to the selected

logic gate, or additionally assigning a bypass condenser cell comprising only a bypass condenser to the selected logic gate.

8. A semiconductor integrated circuit designing apparatus for automatically generating a pattern of a semiconductor integrated circuit under control of a computer, said apparatus comprising:

an input means for inputting net list information of a circuit block as a constituent of a semiconductor integrated circuit, cell library information including bypass condenser cells each comprising at least one bypass condenser for reducing power supply noise and substrate noise, and a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to reduce noise;

a cell arrangement means for arranging cells in a plurality of cell lines that are parallel with each other, according to the net list information;

a comparison means for comparing an on-chip capacitance that is a capacitance of a bypass condenser incorporated in the circuit block, with the capacitance constraint;

a processing ending means for ending the automatic generation of the pattern of the semiconductor integrated circuit when the on-chip capacitance is larger than the capacitance constraint in the comparison by the comparison means; and

a bypass condenser cell addition means for inserting a bypass condenser cell in the cell lines when the on-chip capacitance is equal to or smaller than the capacitance constraint in the comparison by the comparison means.

9. A semiconductor integrated circuit designing method for automatically generating a pattern of a semiconductor integrated circuit under control of a computer, said method comprising:

an input step of inputting gate level logic circuit information, standard cell library information, and package information of a circuit block as a constituent of the semiconductor integrated circuit;

a noise analysis step of performing noise analysis for the circuit block using the inputted information;

a noise judgement step of judging whether the amount of noise that occurs in the circuit block is within a predetermined range or not, on the basis of a result of the noise analysis;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit, when it is judged that the amount of noise is within the predetermined range;

a logic gate selection step of selecting a logic gate in the circuit block, which generates an amount of noise larger than a predetermined amount of noise, when it is judged that the amount of noise in the circuit block is out of the predetermined range;

and

a bypass condenser addition step of adding a bypass condenser for reducing power supply noise and substrate noise to the selected logic gate;

wherein, after the bypass condenser is added in the bypass condenser addition step, processing returns to the noise analysis step, wherein noise analysis is carried out for the circuit block in which the bypass condenser is added.

10. A semiconductor integrated circuit designing method as defined in Claim 9, wherein the noise analysis step creates a data table on which at least one of a current waveform of a power supply current and a current waveform of a substrate current is recorded, which current waveforms are obtained when the input pattern of each logic gate in the circuit block and the capacitance of a bypass condenser incorporated in the logic gate are changed, and performs noise analysis using the created data table.

11. A semiconductor integrated circuit designing method as defined in Claim 9, wherein the logic gate selection step selects a logic gate which generates a maximum amount of noise in the circuit block, on the basis of a result of noise analysis.

12. A semiconductor integrated circuit designing method as

defined in Claim 9, wherein the logic gate selection step calculates a noise influence level which is a degree of influence of noise that occurs in each logic gate in the circuit block, using the inputted information and floor plan information of the semiconductor integrated circuit, and selects a logic gate having a maximum noise influence level.

13. A semiconductor integrated circuit designing method for automatically generating a pattern of a semiconductor integrated circuit under control of a computer, said method comprising:

an input step of inputting gate level logic circuit information, standard cell library information, and package information of a circuit block as a constituent of the semiconductor integrated circuit;

a noise estimation step of estimating an amount of noise that may occur in the circuit block, using the inputted information;

a capacitance constraint designation step of designating a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to restrict the amount of noise within a predetermined range, on the basis of the estimated amount of noise;

a comparison step of comparing an on-chip capacitance that is a capacitance of a bypass condenser incorporated in the circuit block, with the capacitance constraint;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit, when the on-chip capacitance is larger than the capacitance constraint in the comparison step;

a logic gate selection step of selecting a logic gate in the circuit block, which logic gate generates an amount of noise equal to or larger than a predetermined amount of noise, when the on-chip capacitance is equal to or smaller than the capacitance constraint in the comparison step; and

a bypass condenser addition step of adding a bypass condenser to the selected logic gate;

wherein, after the bypass condenser is added in the bypass condenser addition step, the processing returns to the comparison step, wherein the on-chip capacitance that is the capacitance of the bypass condenser incorporated in the circuit block in which the bypass condenser is added is compared with the capacitance constraint.

14. A semiconductor integrated circuit designing method as defined in Claim 13, wherein the logic gate selection step calculates a noise influence level which is a degree of influence of noise that occurs in each logic gate in the circuit block, using the inputted information and floor plan information of the semiconductor integrated circuit, and selects a logic gate having a maximum noise influence level.

15. A semiconductor integrated circuit designing method for automatically generating a pattern of a semiconductor integrated circuit under control of a computer, said method comprising:

an input step of inputting functional specification information of a logic circuit block as a constituent of the semiconductor integrated circuit, standard cell library information of the logic circuit block, and a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to restrict the amount of noise within a predetermined range;

a gate level conversion step of converting the functional specification information of the logic circuit into gate level logic circuit information on the basis of functional levels;

a mapping step of performing a mapping process for assigning cells in the standard cell library information to all logic gates in the gate level logic circuit, respectively;

a comparison step of comparing an on-chip capacitance which is a capacitance of a bypass condenser that is incorporated in the logic circuit subjected to the mapping process, with the capacitance constraint;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit, when the on-chip capacitance is larger than the capacitance constraint in

the comparison step;

a logic gate selection step of selecting a logic gate which generates an amount of noise equal to or larger than a predetermined amount of noise, when the on-chip capacitance is smaller than the capacitance constraint in the comparison step; and

a mapping change step of assigning, in place of the mapping cell assigned in the mapping process, another cell that is equivalent in logic to the mapping cell and has an internal bypass condenser having a different capacitance to the selected logic gate, or additionally assigning a bypass condenser cell comprising only a bypass condenser to the selected logic gate;

wherein, after the other cell is assigned or the bypass condenser cell is additionally assigned in the mapping change step, the processing returns to the comparison step, wherein the on-chip capacitance that is the capacitance of the bypass condenser incorporated in the circuit block in which the other cell is assigned or the bypass condenser cell is additionally assigned, is compared with the capacitance constraint.

16. A semiconductor integrated circuit designing method as defined in Claim 15, wherein the standard cell library information is cell library information to be used for design of the semiconductor integrated circuit, and includes information of at least one set of bypass condenser-incorporated cells having

equivalent logic and different capacitances of the incorporated bypass condensers.

17. A semiconductor integrated circuit designing method for automatically generating a pattern of a semiconductor integrated circuit under control of a computer, said method comprising:

an input step of inputting net list information of a circuit block as a constituent of a semiconductor integrated circuit, cell library information including bypass condenser cells each comprising at least one bypass condenser for reducing power supply noise and substrate noise, and a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to reduce noise;

a cell arrangement step of arranging cells in a plurality of cell lines that are parallel with each other, according to the net list information;

a comparison step of comparing an on-chip capacitance that is a capacitance of a bypass condenser incorporated in the circuit block, with the capacitance constraint;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit when the on-chip capacitance is larger than the capacitance constraint in the comparison step; and

a bypass condenser cell addition step of inserting a bypass

condenser cell in the cell lines when the on-chip capacitance is equal to or smaller than the capacitance constraint in the comparison step;

wherein, after the bypass condenser cell is inserted in the bypass condenser cell addition step, the processing returns to the comparison step, wherein the on-chip capacitance that is the capacitance of the bypass condenser incorporated in the circuit block in which the bypass condenser cell is inserted, is compared with the capacitance constraint.

18. A semiconductor integrated circuit manufacturing method for manufacturing a semiconductor integrated circuit using, for circuit design, a semiconductor integrated circuit designing method for automatically generating a pattern of the semiconductor integrated circuit under control of a computer, said semiconductor integrated circuit designing method comprising:

an input step of inputting gate level logic circuit information, standard cell library information, and package information of a circuit block as a constituent of the semiconductor integrated circuit;

a noise analysis step of performing noise analysis for the circuit block using the inputted information;

a noise judgement step of judging whether the amount of noise that occurs in the circuit block is within a predetermined range

or not, on the basis of a result of the noise analysis;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit, when it is judged that the amount of noise is within the predetermined range;

a logic gate selection step of selecting a logic gate in the circuit block, which generates an amount of noise larger than a predetermined amount of noise, when it is judged that the amount of noise in the circuit block is out of the predetermined range; and

a bypass condenser addition step of adding a bypass condenser for reducing power supply noise and substrate noise to the selected logic gate;

wherein, after the bypass condenser is added in the bypass condenser addition step, the processing returns to the noise analysis step, wherein noise analysis is carried out for the circuit block in which the bypass condenser is added.

19. A semiconductor integrated circuit manufacturing method for manufacturing a semiconductor integrated circuit using, for circuit design, a semiconductor integrated circuit designing method for automatically generating a pattern of the semiconductor integrated circuit under control of a computer, said semiconductor integrated circuit designing method comprising:

an input step of inputting gate level logic circuit information, standard cell library information, and package information of a circuit block as a constituent of the semiconductor integrated circuit;

a noise estimation step of estimating an amount of noise that may occur in the circuit block, using the inputted information;

a capacitance constraint designation step of designating a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to restrict the amount of noise within a predetermined range, on the basis of the estimated amount of noise;

a comparison step of comparing an on-chip capacitance that is a capacitance of a bypass condenser incorporated in the circuit block, with the capacitance constraint;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit, when the on-chip capacitance is larger than the capacitance constraint in the comparison step;

a logic gate selection step of selecting a logic gate in the circuit block, which logic gate generates an amount of noise equal to or larger than a predetermined amount of noise, when the on-chip capacitance is equal to or smaller than the capacitance constraint in the comparison step; and

a bypass condenser addition step of adding a bypass condenser

to the selected logic gate;

wherein, after the bypass condenser is added in the bypass condenser addition step, the processing returns to the comparison step, wherein the on-chip capacitance that is the capacitance of the bypass condenser incorporated in the circuit block in which the bypass condenser is added is compared with the capacitance constraint.

20. A semiconductor integrated circuit manufacturing method for manufacturing a semiconductor integrated circuit using, for circuit design, a semiconductor integrated circuit designing method for automatically generating a pattern of the semiconductor integrated circuit under control of a computer, said semiconductor integrated circuit designing method comprising:

an input step of inputting functional specification information of a logic circuit block as a constituent of the semiconductor integrated circuit, standard cell library information of the logic circuit block, and a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to restrict the amount of noise within a predetermined range;

a gate level conversion step of converting the functional specification information of the logic circuit into gate level

logic circuit information on the basis of functional levels;

a mapping step of performing a mapping process for assigning cells in the standard cell library information to all logic gates in the gate level logic circuit, respectively;

a comparison step of comparing an on-chip capacitance which is a capacitance of a bypass condenser that is incorporated in the logic circuit subjected to the mapping process, with the capacitance constraint;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit, when the on-chip capacitance is larger than the capacitance constraint in the comparison step;

a logic gate selection step of selecting a logic gate which generates an amount of noise equal to or larger than a predetermined amount of noise, when the on-chip capacitance is smaller than the capacitance constraint in the comparison step; and

a mapping change step of assigning, in place of the mapping cell assigned in the mapping process, another cell that is equivalent in logic to the mapping cell and has an internal bypass condenser having a different capacitance to the selected logic gate, or additionally assigning a bypass condenser cell comprising only a bypass condenser to the selected logic gate;

wherein, after the other cell is assigned or the bypass condenser cell is additionally assigned in the mapping change

step, the processing returns to the comparison step, wherein the on-chip capacitance that is the capacitance of the bypass condenser incorporated in the circuit block in which the other cell is assigned or the bypass condenser cell is additionally assigned, is compared with the capacitance constraint.

21. A semiconductor integrated circuit manufacturing method for manufacturing a semiconductor integrated circuit using, for circuit design, a semiconductor integrated circuit designing method for automatically generating a pattern of the semiconductor integrated circuit under control of a computer, said semiconductor integrated circuit designing method comprising:

an input step of inputting net list information of a circuit block as a constituent of a semiconductor integrated circuit, cell library information including bypass condenser cells each comprising at least one bypass condenser for reducing power supply noise and substrate noise, and a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to reduce noise;

a cell arrangement step of arranging cells in a plurality of cell lines that are parallel with each other, according to the net list information;

a comparison step of comparing an on-chip capacitance that is

a capacitance of a bypass condenser incorporated in the circuit block, with the capacitance constraint;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit when the on-chip capacitance is larger than the capacitance constraint in the comparison step; and

a bypass condenser cell addition step of inserting a bypass condenser cell in the cell lines when the on-chip capacitance is equal to or smaller than the capacitance constraint in the comparison step;

wherein, after the bypass condenser cell is inserted in the bypass condenser cell addition step, the processing returns to the comparison step, wherein the on-chip capacitance that is the capacitance of the bypass condenser incorporated in the circuit block in which the bypass condenser cell is inserted, is compared with the capacitance constraint.

22. A readable recording medium in which a semiconductor integrated circuit designing program for making a computer execute processing of designing a semiconductor integrated circuit is computer-readably recorded, said semiconductor integrated circuit designing program comprising:

an input step of inputting gate level logic circuit information, standard cell library information, and package information of a circuit block as a constituent of the

semiconductor integrated circuit;

a noise analysis step of performing noise analysis for the circuit block using the inputted information;

a noise judgement step of judging whether the amount of noise that occurs in the circuit block is within a predetermined range or not, on the basis of a result of the noise analysis;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit, when it is judged that the amount of noise is within the predetermined range;

a logic gate selection step of selecting a logic gate in the circuit block, which generates an amount of noise larger than a predetermined amount of noise, when it is judged that the amount of noise in the circuit block is out of the predetermined range; and

a bypass condenser addition step of adding a bypass condenser for reducing power supply noise and substrate noise to the selected logic gate;

wherein, after the bypass condenser is added in the bypass condenser addition step, the processing returns to the noise analysis step, wherein noise analysis is carried out for the circuit block in which the bypass condenser is added.

23. A readable recording medium in which a semiconductor integrated circuit designing program for making a computer

execute processing of designing a semiconductor integrated circuit is computer-readably recorded, said semiconductor integrated circuit designing program comprising:

an input step of inputting gate level logic circuit information, standard cell library information, and package information of a circuit block as a constituent of the semiconductor integrated circuit;

a noise estimation step of estimating an amount of noise that may occur in the circuit block, using the inputted information;

a capacitance constraint designation step of designating a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to restrict the amount of noise within a predetermined range, on the basis of the estimated amount of noise;

a comparison step of comparing an on-chip capacitance that is a capacitance of a bypass condenser incorporated in the circuit block, with the capacitance constraint;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit, when the on-chip capacitance is larger than the capacitance constraint in the comparison step;

a logic gate selection step of selecting a logic gate in the circuit block, which logic gate generates an amount of noise equal to or larger than a predetermined amount of noise, when the

on-chip capacitance is equal to or smaller than the capacitance constraint in the comparison step; and

a bypass condenser addition step of adding a bypass condenser to the selected logic gate;

wherein, after the bypass condenser is added in the bypass condenser addition step, the processing returns to the comparison step, wherein the on-chip capacitance that is the capacitance of the bypass condenser incorporated in the circuit block in which the bypass condenser is added is compared with the capacitance constraint.

24. A readable recording medium in which a semiconductor integrated circuit designing program for making a computer execute processing of designing a semiconductor integrated circuit is computer-readably recorded, said semiconductor integrated circuit designing program comprising:

an input step of inputting functional specification information of a logic circuit block as a constituent of the semiconductor integrated circuit, standard cell library information of the logic circuit block, and a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to restrict the amount of noise within a predetermined range;

a gate level conversion step of converting the functional

specification information of the logic circuit into gate level logic circuit information on the basis of functional levels;

a mapping step of performing a mapping process for assigning cells in the standard cell library information to all logic gates in the gate level logic circuit, respectively;

a comparison step of comparing an on-chip capacitance which is a capacitance of a bypass condenser that is incorporated in the logic circuit subjected to the mapping process, with the capacitance constraint;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit, when the on-chip capacitance is larger than the capacitance constraint in the comparison step;

a logic gate selection step of selecting a logic gate which generates an amount of noise equal to or larger than a predetermined amount of noise, when the on-chip capacitance is smaller than the capacitance constraint in the comparison step; and

a mapping change step of assigning, in place of the mapping cell assigned in the mapping process, another cell that is equivalent in logic to the mapping cell and has an internal bypass condenser having a different capacitance to the selected logic gate, or additionally assigning a bypass condenser cell comprising only a bypass condenser to the selected logic gate;

wherein, after the other cell is assigned or the bypass

condenser cell is additionally assigned in the mapping change step, the processing returns to the comparison step, wherein the on-chip capacitance that is the capacitance of the bypass condenser incorporated in the circuit block in which the other cell is assigned or the bypass condenser cell is additionally assigned, is compared with the capacitance constraint.

25. A readable recording medium in which a semiconductor integrated circuit designing program for making a computer execute processing of designing a semiconductor integrated circuit is computer-readably recorded, said semiconductor integrated circuit designing program comprising:

an input step of inputting net list information of a circuit block as a constituent of a semiconductor integrated circuit, cell library information including bypass condenser cells each comprising at least one bypass condenser for reducing power supply noise and substrate noise, and a capacitance constraint that is a capacitance of a bypass condenser for reducing power supply noise and substrate noise, which bypass condenser is to be incorporated in the circuit block to reduce noise;

a cell arrangement step of arranging cells in a plurality of cell lines that are parallel with each other, according to the net list information;

a comparison step of comparing an on-chip capacitance that is a capacitance of a bypass condenser incorporated in the circuit

block, with the capacitance constraint;

a processing ending step of ending the automatic generation of the pattern of the semiconductor integrated circuit when the on-chip capacitance is larger than the capacitance constraint in the comparison step; and

a bypass condenser cell addition step of inserting a bypass condenser cell in the cell lines when the on-chip capacitance is equal to or smaller than the capacitance constraint in the comparison step;

wherein, after the bypass condenser cell is inserted in the bypass condenser cell addition step, the processing returns to the comparison step, wherein the on-chip capacitance that is the capacitance of the bypass condenser incorporated in the circuit block in which the bypass condenser cell is inserted, is compared with the capacitance constraint.